IN THE CLAIMS

Please take action regarding the claims so that the status is as follows:

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Currently Amended) In a data processing system having a processor responsively coupled to a store-in cache memory which is responsively coupled to a lower level memory, the improvement comprising:

a. a read-only level one instruction cache memory directly coupled to said processor;

b. a store-through level one operand cache memory directly coupled to said processor;

c. wherein said processor is responsively coupled to said store-in cache memory via said read-only level one instruction cache memory and via said store-through level one operand cache memory; d. a flush buffer directly coupled to said store-in cache memory and said lower level memory;

e. a tag memory responsively coupled to said store-in cache memory which indicates whether a particular location within said store-in memory has been modified by said processor;

f. a logic circuit which loads said flush buffer with data from said particular location within said store-in cache memory in response to said indication that said particular location within said store-in memory has been modified by said processor; and

g. ~~according to claim 3~~ wherein said flush buffer further comprises a first flush buffer store having a first input responsively coupled to said store-in cache memory and a first output directly coupled to said lower level memory and a second flush buffer store having a second input responsively coupled to said store-in cache memory and a second output directly coupled to said lower level memory.

5. (Original) A data processing system according to claim 4 further comprising a temporary register responsively coupled to said store-in cache memory, said first flush buffer store, and said second flush buffer store which routes said data from said particular location to an available one of said first flush buffer store and said second flush buffer store.

6. (Canceled)

7. (Currently Amended) A data processing system ~~according to claim 6~~ comprising:

a. A processor;

b. A level one store-through cache memory having a read-only instruction portion and an operand portion directly coupled to said processor;

c. A store-in cache memory responsively coupled to said processor via said read-only instruction portion and said operand portion of said level one store-through cache memory;

d. A lower level memory responsively coupled to said store-in cache memory;

e. A flush buffer directly coupled to said store-in cache memory and said lower level memory; and

f. wherein said flush buffer further comprises a first flush buffer store having a first input responsively coupled to said store-in cache memory and a first output directly coupled to said lower level memory and a second flush buffer store having a second input responsively coupled to said store-in cache memory and a second output directly coupled to said lower level memory.

8. (Original) A data processing system according to claim 7 further comprising:

a. A temporary register responsively coupled to said store-in cache memory, said first flush buffer store, and said second flush buffer store.

9. (Original) A data processing system according to claim 8 further comprising:

a. A tag memory responsively coupled to said store-in cache memory for indicating whether a particular location has been modified by said processor.

10. (Previously Presented) A data processing system according to claim 9 further comprising:

a. A logic circuit responsively coupled to said tag memory, said store-in cache memory, and said temporary register which routes data from said particular location from said store-in cache memory to said temporary register when said indication is that said particular location has been modified by said processor.

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)